**North SouthUniversity**

Department of Computer Science and Engineering

**Final**,Summer-2017

Course No: **CSE332** Course Title: **Computer Organization and Design**

Time:50 min Full Marks:40

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| 1. | Identify the differences between multi cycle and pipeline datapath. | 3 |
| 2. | Explain data hazard with a specific example. | 2 |
| 3. | Consider the following table that provides the time required by each of the 5 stage of two different processor a and b.   |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | **Processor** | **Instr. Fetch**  (ps) | **Instr. Decode**  (ps) | **EX**  (ps) | **Mem**  (ps) | **Write Back**  (ps) | | **a** | 300 | 400 | 250 | 500 | 100 | | **b** | 220 | 200 | 100 | 150 | 80 |   Identify the following for multi cycle and pipelined version of the datapath for both processors.   * Clock cycle time(Tc) * Time between two consecutive instructions * Number of instructions that can be executed per (Calculate this based on the above set of instructions only) * Calculate throughput 10 instructions (5 of them lw type, 5 of them add type) | 12 |
| 4. | Consider the following MIPS assembly code and assume that we are using pipeline processor. Now answer following questions.  a. Locate the hazards (if any) into the codes. (use circle to locate)  b. How can you solve those?  c. What is the number of clock cycles required to perform the code correctly? Calculate based on your proposed solution in 4b)  d. Is rescheduling possible? if yes, how many clock cycles requiredafter rescheduling  lw$t1, 0($t0)  and $t3, $t1, $t2  sub $t4, $t1, $t3  slt $t0, $t4, $t3 | 10 |
| 5. | The following datapath diagram is missing all the control signal lines. Identify them all by labeling. | 3 |
| 6. | The instruction formats for a particular 10 bit ISA are provided as below.  **R-type**  *MSB LSB*   |  |  |  |  |  | | --- | --- | --- | --- | --- | | op (2 bit) | rt (2 bit) | rs (2 bit) | rd (2 bit) | func (2 bit) |   **I-type**   |  |  |  |  | | --- | --- | --- | --- | | op (2 bit) | rt (2 bit) | rs (2 bit) | immediate (4 bit) |   Consider the following set of compiled instructions that will be run into this ISA.  *lw $t1, 0 ($t0) (1)*  *lw $t2, 0($t0) (2)*  *add $t2,$t1,$t2 (3)*  *sw $t2, 0($t0) (4)*  *Now answer the following questions :*  a. Draw a complete single cycle datapath that can perform the above instructions. Show the connectivity, the bus width of the connections (in bits)s  b. The above single cycle datapath has been divided into 3 stages (IF,ID,EX,MEM,WB) for improving the performance through pipelining. This has been done by adding few pipelines registers in between the stages. How many of the pipeline registers are required? Calculate the width of pipeline registers?  c. draw the pipelined version of the datapath | 10 |
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